

Inventor: John T. Moore et al.

Title: Semiconductor Wafer Assemblies Comprising Photoresist Over Silicon Nitride Materials

Assignee: Micron Technology, Inc.

**INFORMATION DISCLOSURE STATEMENT**  
**PURSUANT TO 37 C.F.R. " 1.56, 1.97 AND 1.98**

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

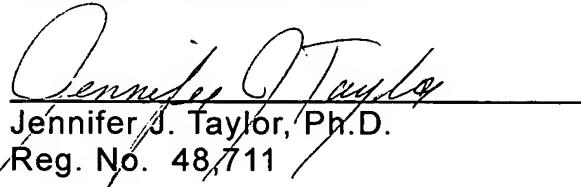
The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a continuation application of co-pending application Serial No. 09/995,372, filed November 26, 2001. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2).

Citation of these references is respectfully requested.

Dated: December 11, 2003

By:

Respectfully submitted,

  
Jennifer J. Taylor, Ph.D.  
Reg. No. 48,711

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2463	PRIORITY SERIAL NO. 09/995,372		
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT John T. Moore et al.			
				PRIORITY FILING DATE November 26, 2001		PRIORITY GROUP 2815	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,219,788	6/93	Abernathey et al.			
	AB	5,045,847	9/91	Tarui et al.			
	AC	5,045,345	9/91	Singer			
	AD	4,996,081	2/91	Ellul et al.			
	AE	3,884,698	5/75	Kakihama et al.			
	AF	5,518,946	5/96	Kuroda			
	AG	5,489,542	2/96	Iwai et al.			
	AH	4,330,569	5/82	Gulett et al.			
	AI	4,499,656	2/85	Fabian et al.			
	AJ	5,554,418	9/96	Ito et al.			
	AK	5,926,739	7/99	Rolfson et al.			
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes      No
	AL	401086562	3/89	Japan			
	AM	362137854	6/87	Japan			
	AN	2129217	5/84	Great Britain			
	AO	2170649	8/86	Great Britain			
	AP	2145243	3/85	Great Britain			
	AQ	403075158	3/91	Japan			
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AR		Silicon Proc. for VLSI; 177-178; Vol. 1; S. Wolf				
	AS		Silicon Proc. for VLSI; 191-193; Vol. 1; S. Wolf				
EXAMINER				DATE CONSIDERED			
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>							

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U.S. PATENT DOCUMENTS								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	4,874,716	10/89	Rao				
	AB	5,587,344	12/96	Ishikawa				
	AC	4,439,270	3/84	Powell et al.				
	AD	5,773,325	6/98	Teramoto				
	AE	5,904,523	5/99	Feldman et al.				
	AF	5,891,793	4/99	Gardner et al.				
	AG	5,795,821	8/98	Bacchetta et al.				
	AH	5,918,147	6/99	Filipiak et al.				
	AI	5,882,978	3/99	Srinivasan et al.				
	AJ	4,612,629	9/86	Harari				
	AK	5,831,321	11/98	Nagayama				
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							Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							
	AQ							
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)								
	AR		Silicon Proc. for VLSI; 37-38; 598-599; Vol. 2; S. Wolf					
	AS		Electronic Materials Science: For Integrated Circuits; 1990 ©; Mayer et al; pp. 269-274; Pub. 1990					
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	3,549,411	12/70	Bean			
	AB	4,446,194	5/84	Candelaria			
	AC	4,485,553	12/84	Christian			
	AD	4,543,707	10/85	Ito et al.			
	AE	5,098,865	3/92	Machado et al.			
	AF	5,160,998	11/92	Itoh et al.			
	AG	5,306,946	4/94	Yamamoto			
	AH	5,442,223	8/95	Fujii			
	AI	5,523,616	6/96	Den			
	AJ	5,756,404	5/98	Friedenreich et al.			
	AK	5,834,374	11/98	Cabral Jr. et al.			
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	AL						Yes
	AM						No
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	AO						
	AP						
	AQ						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AR		Intrinsic Stress in Silicon Nitride and Silicon Dioxide Films Prepared by Various Deposition Techniques; 1988 IEEE Internat'l. Sympos. On Electrical Insulation, Boston, MA; June 5-8, 1988; 1 page; Kanicki, J. et al.				
	AS		Passivation of GaAsFET's with PECVD Silicon Nitride Films of Different Stress States; IEEE Transactions on Electron Devices; Vol. 35, No. 9; Sept. 1988; pp. 1412-1418				
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	4,695,872	9/87	Chatterjee				
	AB	5,178,016	1/93	Dauenhauer et al.				
	AC	5,985,771	11/99	Moore et al.				
	AD	3,649,884	3/72	Haneta				
	AE	4,868,632	9/89	Hayashi				
	AF	5,304,829	4/94	Mori et al.				
	AG	5,925,494	7/99	Horn				
	AH	4,075,367	2/78	Gulett				
	AI	4,732,858	3/88	Brewer et al.				
	AJ	6,300,253	10/01	Moore, John T.				
	AK	4,698,787	10/87	Mukherjee et al.				
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)								
	AR		Silicon Nitride Overcoats for Thin Film Magnetic Recording Media; IEEE Transactions on Magnetics; Vol 27. No. 6, Nov. 1991; pp. 5070-5072					
	AS							
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	AA	4,939,559	07/90	DiMaria et al.			
	AB	6,140,181	10/00	Forbes et al.			
	AC	6,143,627	11/00	Robinson			
	AD	5,877,069	03/99	Robinson			
	AE	6,093,956	07/00	Moore et al.			
	AF	6,103,619	08/00	Lai			
	AG	6,265,241	07/01	Pan			
	AH	6,420,777		Lam et al.			
	AI	6,417,559	07/02	Moore et al.			
	AJ	5,041,888	08/91	Possin et al.			
	AK	6,143,662	11/00	Rhodes et al.			
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	AN						
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